

FIG. 1

BEST AVAILABLE COPY

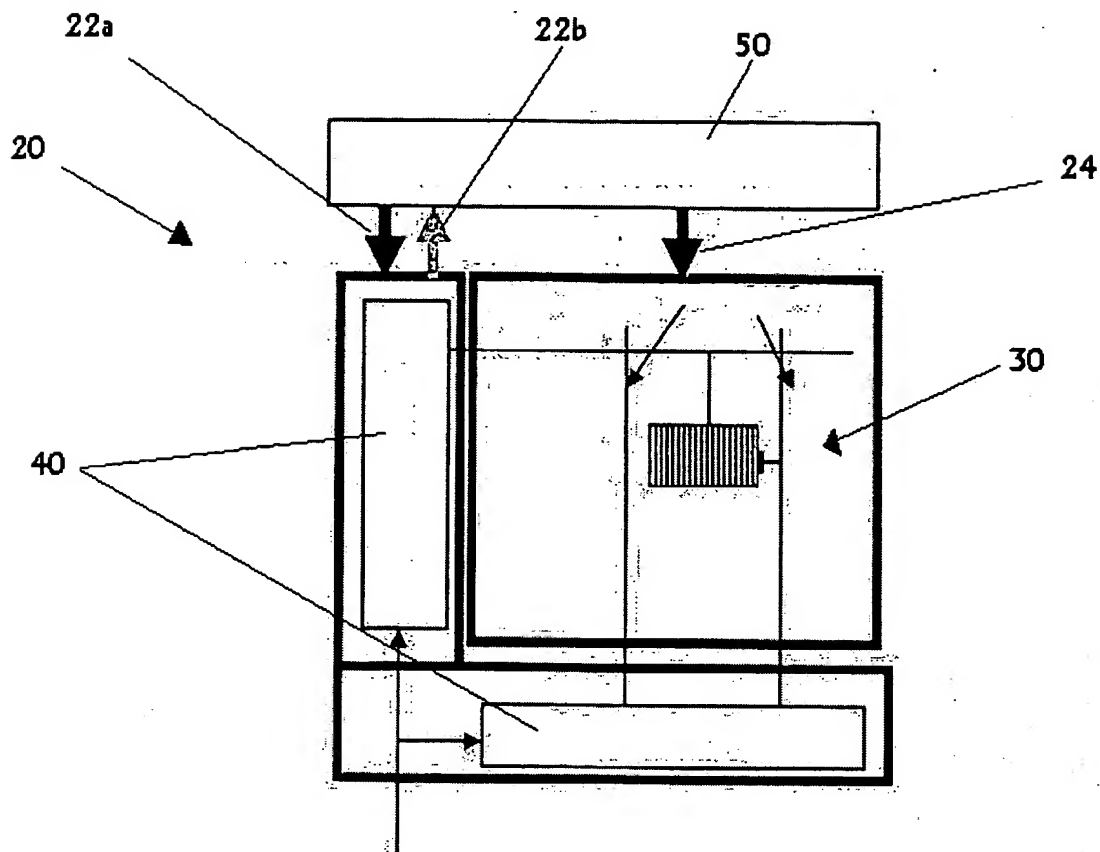


FIG. 2

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Memory Name: [L2RAM1-100]

Number of Words: [8192]
Number of Bits: [32]
Column-Mux Option: [16]
Frequency (MHz): [10]
Layer Standard File: [70uhmno/suchin] [Browse...]
Metal Layers in Product: [5]
Support Top Via: ☐ Yes ☒ No
Ultra low power: ☒ Yes ☐ No

Ring Test Options:
Lower Left: ☒ Yes ☐ No
Lower Right: ☒ Yes ☐ No
Upper Left: ☒ Yes ☐ No
Upper Right: ☒ Yes ☐ No
Netlist File Options:
Viasing Brackets: ☒ Yes ☐ No
Splice Brackets: ☒ Yes ☐ No

Ring Ratio:
Left: [1.0] Right: [1.0] Top: [1.0]
Width: [20.0] [Auto]

Pin Routing Layer: [MET1]
Metal Layer: Signal
Internal: [MET0] [VSS]
External: [MET3] [VDD]

Power Ring:
Ring Placement Type:
Type1: describe...
Type2: describe...
Type3: describe...

Table:
Name: [V]
F: [1.50] 25.0 Typ: [99.1]
P: [1.45] 0.0 Fast
S: [1.25] 125.0 Slow

New Edit Delete

OK Cancel

Valid Range: 1 to 700

62 →
64 →
60 →

FIG. 3

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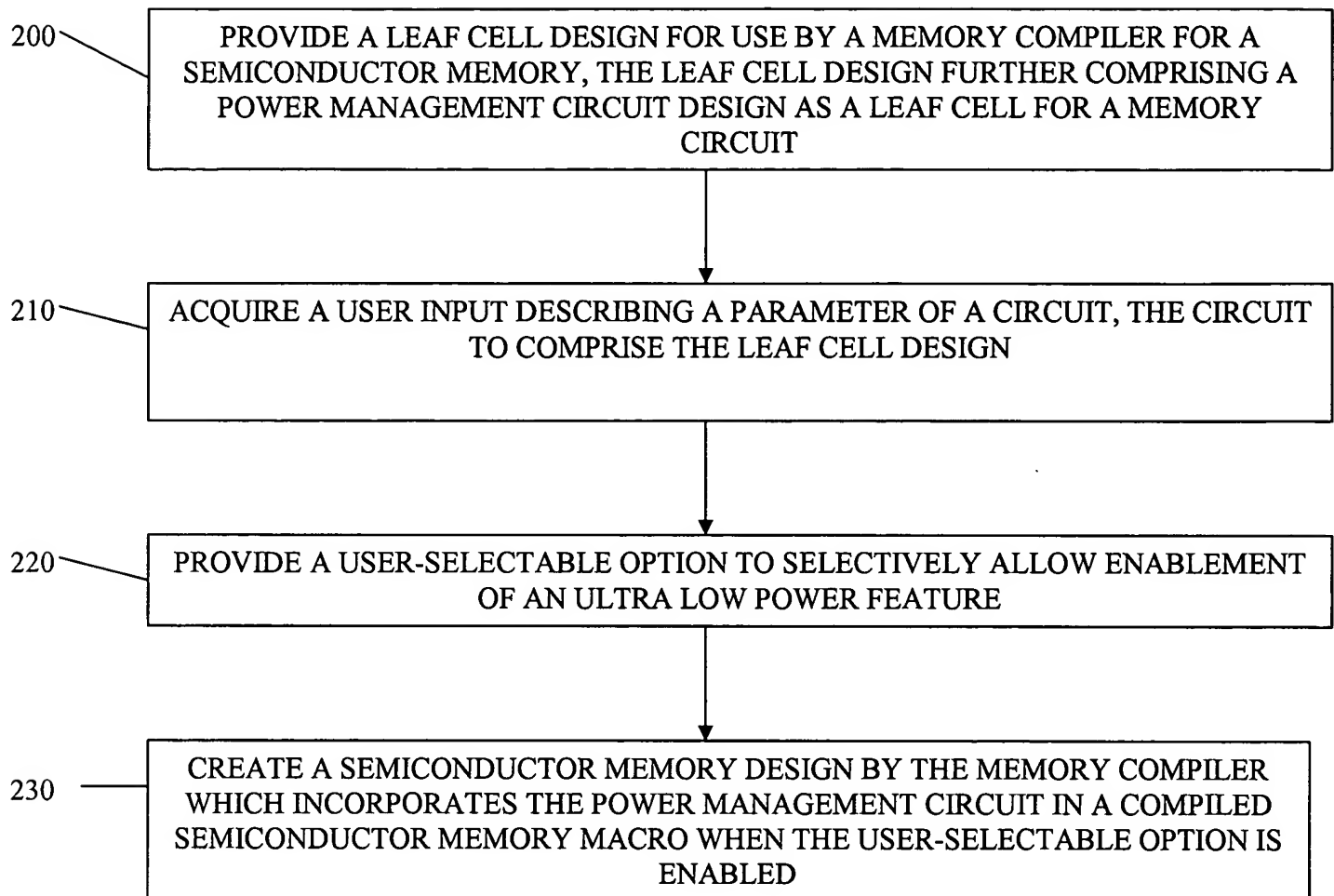


FIG. 4